

WHAT IS CLAIMED IS:

1 1. A data processor having a clustered architecture
2 comprising:

3 a branching cluster and a non-branching cluster, each
4 capable of computing branch conditions, said branching cluster
5 operable to perform branch address computations for said branching
6 cluster and said non-branching cluster; and

7 remote conditional branching control circuitry that
8 causes said branching cluster to perform a branch address
9 computation in response to sensing a conditional branch instruction
10 in said non-branching cluster, and that communicates a computed
11 branch condition from said non-branching cluster to said branching
12 cluster.

13 2. The data processor as set forth in Claim 1 wherein each
14 of said branching cluster and said non-branching cluster comprises
15 at least one register file.
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1 3. The data processor as set forth in Claim 1 wherein each
2 of said branching cluster and said non-branching cluster comprises
3 an instruction execution pipeline comprising N processing stages,
4 each of said N processing stages capable of performing at least one
5 of a plurality of execution steps associated with a pending
6 instruction being executed by said instruction execution pipeline.

1 4. The data processor as set forth in Claim 1 wherein said
2 remote conditional branching control circuitry further causes said
3 branching cluster to perform a next program counter address
4 computation in response to sensing a conditional branch instruction
5 in said non-branching cluster.

1 5. The data processor as set forth in Claim 4 wherein said
2 remote conditional branching control circuitry selects one of said
3 computed next program counter address and said computed branch
4 address in response to said computed branch condition.

1 6. The data processor as set forth in Claim 5 wherein said
2 remote conditional branching control circuitry comprises a
3 multiplexor that is responsive to said computed branch condition.

1 7. The data processor as set forth in Claim 1 wherein said
2 data processor issues a shadow conditional branch instruction in
3 said branching cluster to perform said branch address computation
4 in response to sensing said conditional branch instruction in said
5 non-branching cluster.

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1 8. For use in a data processor comprising at least a
2 branching cluster and a non-branching cluster, each capable of
3 computing branch conditions, said branching cluster operable to
4 perform branch address computations for said branching cluster and
5 said non-branching cluster, a method of operating said data
6 processor comprising the steps of:

7 computing a branch address in response to sensing a
8 conditional branch instruction in said non-branching cluster; and
9 communicating a branch condition computed by said non-
10 branching cluster from said non-branching cluster to said branching
11 cluster.

12 9. The method of operating said data processor as set forth
13 in Claim 8 further comprising the step of computing said branch
14 condition in said non-branching cluster.

15 10. The method of operating said data processor as set forth
16 in Claim 9 further comprising the step of computing a next program
17 counter address.

1 11. The method of operating said data processor as set forth
2 in Claim 10 further comprising the step of selecting one of said
3 computed next program counter address and said computed branch
4 address in response to said computed branch condition.

1 12. The method of operating said data processor as set forth
2 in Claim 8 wherein each of said branching cluster and said non-
3 branching cluster comprises an instruction execution pipeline
4 comprising N processing stages, said method further comprising the
5 step of performing in each of said N processing stages at least one
6 of a plurality of execution steps associated with a pending
7 instruction being executed by said instruction execution pipeline.

1 13. The method of operating said data processor as set forth
2 in Claim 8 further comprising the step of issuing a shadow
3 conditional branch instruction in said branching cluster to perform
4 said branch address computation in response to sensing said
5 conditional branch instruction in said non-branching cluster.

1 14. A processing system comprising:
2 a data processor having a clustered architecture;
3 a memory associated with said data processor;
4 a plurality of peripheral circuits associated with said
5 data processor for performing selected functions in association
6 with said data processor, wherein said data processor comprises:
7 at least a branching cluster and a non-branching
8 cluster that are capable of computing branch conditions, said
9 branching cluster operable to perform branch address
10 computations for said at least said branching cluster and said
11 non-branching cluster; and
12 remote conditional branching control circuitry that
13 causes said branching cluster to perform a branch address
14 computation in response to sensing a conditional branch
15 instruction in said non-branching cluster, and that
16 communicates a computed branch condition from said non-
17 branching cluster to said branching cluster.

1 15. The processing system as set forth in Claim 14 wherein
2 each of said branching cluster and said non-branching cluster
3 comprises at least one register file.

1 16. The processing system as set forth in Claim 14 wherein
2 each of said at least said branching cluster and said non-branching
3 cluster comprises an instruction execution pipeline comprising N
4 processing stages, each of said N processing stages capable of
5 performing at least one of a plurality of execution steps
6 associated with a pending instruction being executed by said
7 instruction execution pipeline.

8 17. The processing system as set forth in Claim 14 wherein
9 said remote conditional branching control circuitry further causes
10 said branching cluster to perform a next program counter address
11 computation in response to sensing a conditional branch instruction
12 in said non-branching cluster.

13 18. The processing system as set forth in Claim 17 wherein
14 said remote conditional branching control circuitry selects one of
15 said computed next program counter address and said computed branch
16 address in response to said computed branch condition.

1 19. The processing system as set forth in Claim 18 wherein
2 said remote conditional branching control circuitry comprises a
3 multiplexor having an input channel associated with said non-
4 branching cluster, said multiplexor responsive to said computed
5 branch condition.

1 20. The processing system as set forth in Claim 14 wherein
2 said data processor issues a shadow conditional branch instruction
3 in said branching cluster to perform said branch address
4 computation in response to sensing said conditional branch
5 instruction in said non-branching cluster.